

**AMENDMENTS TO THE CLAIMS**

1. (Currently Amended) A method comprising:
- executing a first instruction in a processor;
- if the execution of the first instruction generates a cache miss, associating the first instruction with the cache miss;
- associating the cache miss with a second instruction dependent on the first instruction;
- enqueueing the first instruction for re-execution; ~~and~~
- enqueueing the second instruction for execution; and
- after the cache miss with which the first instruction is associated is serviced, re-executing the first instruction and executing the second instruction.

- Do  
Not Enter -  
BGP  
10/1/07

2. (Canceled)
3. (Original) The method of claim 1, further comprising assigning an identifier to the cache miss.
4. (Original) The method of claim 1, further comprising determining a priority of the instruction.
5. (Currently Amended) A processor comprising: a re-scheduler to hold instructions enqueueued for execution;